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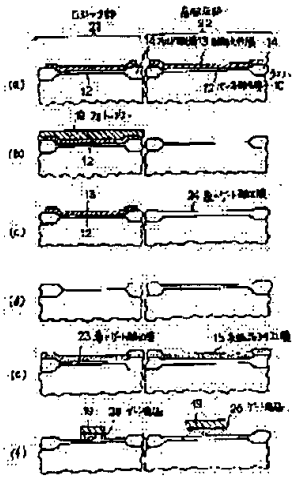
(54) FABRICATION OF MOS TYPE INTEGRATED CIRCUIT DEVICE

(57)Abstract:
PURPOSE: To deposit gate oxides with different thickness on the wafer of an integrated circuit device while protecting the wafer against contamination with a photoresist resin during photoprocess.
CONSTITUTION: Under a state where the part for depositing gate oxides 23, 24 on the surface of a wafer 10 is covered entirely with an anti-oxidation film 13, e.g. silicon nitride, a field oxide 14 is provided through selective oxidation. The anti-oxidation film 13 is then removed from the part for depositing the gate oxide 24 by photoetching. In other words, a thick gate oxide 24 is deposited by thermal oxidation while covering the part for deposition the thin gate oxide 23 with the anti-oxidation film 13. Furthermore, under a state where the anti-oxidation film 13 is removed entirely from the surface of the wafer 10, the thin gate oxide 23 is deposited by thermal oxidation and then the thick gate oxide 24 is deposited thereon. Consequently, the gate oxides 23, 24 having different thickness are deposited for the transistors 41, 42 at a logic part 21 and a high breakdown strength part 22.



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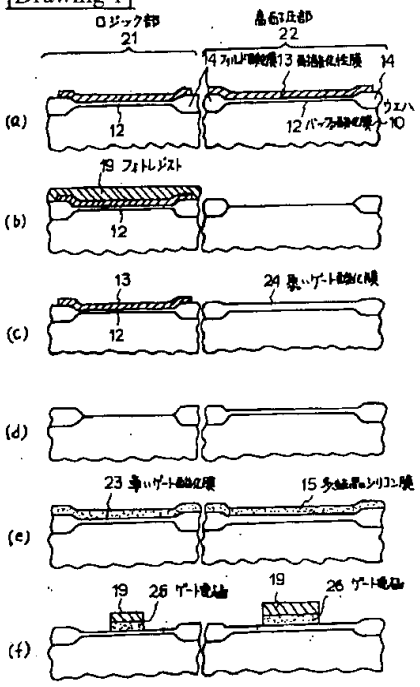
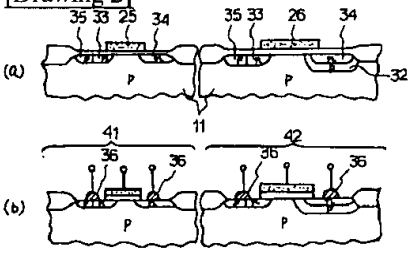
* NOTICES *

DRAWINGS

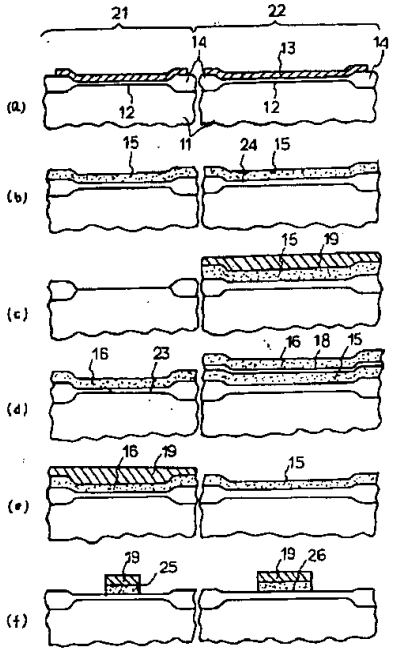
[Drawing 1]



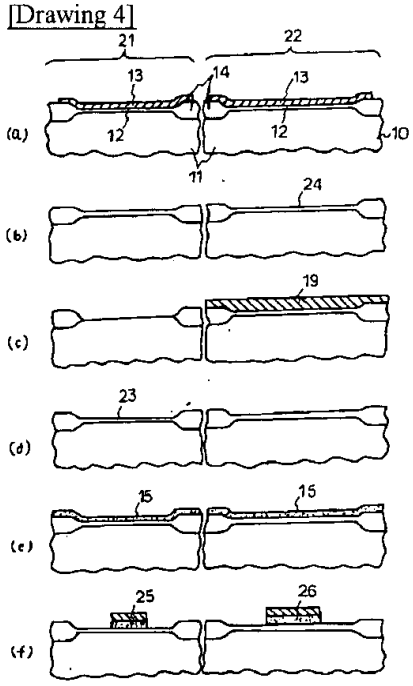
[Drawing 2]



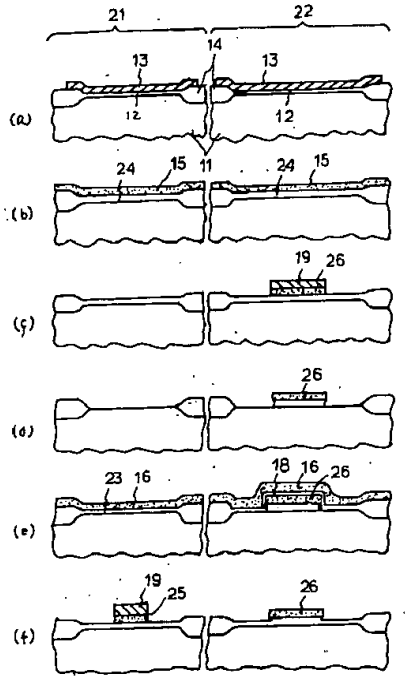
[Drawing 3]



[Drawing 4]



[Drawing 5]



[Translation done.]

* NOTICES *

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] (a) It is a cross section for every main process to the gate electrode formation for explaining the manufacture method of the MOS type integrated circuit device which there is not and (f) requires for this invention.
[Drawing 2] (a) It is a cross section for every main process for reaching and (b) explaining the manufacture method of the MOS type integrated circuit device concerning this invention following drawing 1 .
[Drawing 3] (a) It is a cross section for every main process to the gate electrode formation for explaining the another manufacture method of the MOS type integrated circuit device which there is not and (f) requires for this invention.
[Drawing 4] (a) It is a cross section for every main process to the gate electrode formation for there being nothing and (f) explaining the manufacture method of the conventional MOS type integrated circuit device.
[Drawing 5] (a) It is a cross section for every main process to the gate electrode formation for there being nothing and (f) explaining the another manufacture method of the conventional MOS type integrated circuit device.
[Description of Notations]
10 Wafer
11 Semiconductor Region
12 Buffer Oxide Film
13 Oxidation-resistant Film
14 Field Oxide Film
15 First Polycrystal Silicon Film
16 Second Polycrystal Silicon Film
17 First Oxide Film
18 Polycrystal Silicon Film Top Oxide Film
19 Photoresist
21 Logic Section
22 High Pressure Part
23 Thin Gate Oxide Film
24 Thick Gate Oxide Film
25 Gate Electrode
26 Gate Electrode
32 N Type Low Concentration Field
33 N Type Source Field
34 N Type Drain Field
35 P Type Contact Field
36 Electrode
41 MOS Transistor of Logic Section
42 MOS Transistor of High Pressure Part

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] this invention relates to the manufacture method of the MOS type integrated circuit device which accumulated a mutually different MOS type semiconductor device of operating voltage, especially the MOS type semiconductor device which has the gate oxide film from which thickness differs mutually on the semiconductor chip of a piece.
[0002]
[Description of the Prior Art] The technology which creates high pressure-proofing, mass circuit element, and the circuit element of small capacity suitable for high-speed operation aiming at the drive of a load is becoming important comparatively in the same chip with expansion of the use of an integrated circuit device. In this integrated circuit device, the circuit element for a load drive (this circuit element is called a high pressure part below) usually under the supply voltage of 40-60V Moreover, since the circuit element for high-speed operations (this circuit element is called the logic section below) usually operates under the low-pressure control-power-source voltage of 5V It is necessary to give the pressure-proofing according to the operating voltage to each circuit element, and when circuit element is an insulating gate control type element, it is necessary to give the thickness according to the required pressure-proofing concerning the gate oxide film. For example, although the thickness of the gate oxide film of the logic section is 25-40nm in order to make high-speed operation of the logic section possible, since the voltage of 40-60V is impressed also to a gate oxide film about a high pressure part, the thickness of 130-150nm is required for the gate oxide film of a quantity pressure part. Therefore, it is required for such a wafer for integrated circuit devices to form two kinds of gate oxide films from which thickness differs mutually.
[0003] Drawing 4 shows the conventional method until the thickness of such a wafer for integrated circuit devices forms a gate electrode on two kinds of mutually different gate oxide films with the cross section for every main processes. In drawing 4 (a), the semiconductor regions 11 of a wafer 10 are a semiconductor substrate, an epitaxial layer, and a well. It is a cross section in the state where it was formed so that each range from which the field oxide film 14 for isolation should make a semiconductor device to one principal plane of a wafer 10 might be surrounded with the conventional selective oxidation technology. 12 is a buffer oxide film and the oxidation-resistant film [like a silicon nitride film] whose 13 is. The left-hand side of drawing is the portion which should form a gate oxide film with right-hand side thick at the high pressure part 22 for a gate oxide film thin in the logic section 21, respectively.
[0004] Next, after removing the oxidation-resistant film 13 and the buffer oxide film 12, the thick gate oxide film 24 is first formed by 900 degrees C and PAIRO oxidization for about 57 minutes all over a wafer (the range on the left-hand side of drawing which should form a thin gate oxide film is included) 10 [drawing 4 (b)]. At this process, membranes are formed to 135nm thinner thickness to set the last thickness of the gate oxide film 24 of a high pressure part to about 150nm.
[0005] Then, the high pressure part 22 on the right-hand side of drawing is covered by the photoresist 19, for example, the thick oxide film 24 of the logic section 21 on the left-hand side of drawing which is not covered by the photoresist 19 is removed by the wet etching using rare fluoric acid, and the front face of a semiconductor region 11 is exposed [drawing 4 (c)]. Furthermore, after ashing and remover liquid remove a photoresist 19 from the front face of a wafer 10, 800 degrees C and PAIRO oxidization for about 40 minutes are performed. Thereby, the thin gate oxide film 23 with a thickness of about 25nm is formed by the logic section 21. Moreover, although the thick gate oxide film 24 stacks and it increases, since the high pressure part 22 on the right-hand side of drawing is also oxidized thermally simultaneously with this, since the growth rate of the oxide film at the time of thermal oxidation falls in the increase in thickness, only 15nm of thick gate oxide films 24 is stacked, and it increases, and it becomes thickness almost equal to 150nm of a target [drawing 4 (d)]. The growth rates of a gate oxide film differ by the logic section 21 and the high pressure part 22 here for going on with the oxidization kind with which oxidation reaction has diffused the inside of an oxide film in the interface of an oxide film and a silicon substrate. Therefore, it becomes difficult for an oxidization kind to reach the interface of an oxide film and a silicon substrate as an oxide film becomes thick, and a growth rate becomes slow.
[0006] Then, the polycrystal silicon film 15 is deposited all over a wafer 10 by reduced pressure CVD [drawing 4 (e)]. furthermore, photo etching technology -- the thin gate oxide-film 23 top -- the gate electrode 25 of the logic section -- moreover, drawing 4 (f)] which forms the gate electrode 26 of the thick gate oxide-film 24 top quantity pressure part
[0007] Drawing 5 shows an option until the thickness of the wafer for integrated circuit devices forms a gate electrode on two kinds of mutually different gate oxide films with the cross section for every main processes. drawing 5 (a) is a cross section in the

state where it was formed so that each range from which the field oxide film 14 of the well of isolation should make a semiconductor device to one principal plane of a wafer 10 might be surrounded with selective oxidation technology as well as drawing 4 (a) 12 is a buffer oxide film and the oxidation-resistant film [like a silicon nitride film] whose 13 is. The left-hand side of drawing is the portion which should form a gate oxide film with right-hand side thick at the high pressure part 22 for a gate oxide film thin in the logic section 21, respectively.

[0008] First, after removing the oxidation-resistant film 13 and the buffer oxide film 12, all over a wafer 10, the thick gate oxide film 24 with a thickness of 150nm is formed by 900 degrees C and PAIRO oxidization for about 61 minutes, and the first polycrystal silicon film 15 is continuously deposited all over a wafer 11 by reduced pressure CVD [drawing 5 (b)]. Next, pattern formation of the photoresist 19 is applied and carried out, and the gate electrode 26 of the high pressure part 22 is formed [drawing 5 (c)].

[0009] Furthermore, in the high pressure part 22, although the thick gate oxide film 24 of the logic section 21 will be removed and the front face of a semiconductor region 11 will be exposed if complete etching by fluoric acid is performed after ashing and remover liquid remove a photoresist 19 from the front face of a wafer 10, the thick oxide film 24 under the gate electrode 26 remains without **********ing [drawing 5 (d)].

[0010] 800 degrees C of second gate oxidization are performed after an appropriate time about 40 minutes, and about 25nm of thin gate oxide films 23 of the logic section 21 is formed. At this time, the gate electrode 26 of the quantity pressure part 22 also oxidizes, and an oxide film 18 is formed on the gate electrode 26. Then, the second polycrystal silicon film 16 is deposited on the whole surface [drawing 5 (e)]. Furthermore, a photoresist 19 is applied and the gate electrode 25 of the logic section is formed on the thin gate oxide film 23 of the logic section 21 with photo etching technology. Etching removal of the second polycrystal silicon film 16 on the high pressure part 22 is carried out simultaneously. At this time, the oxide film 18 on the gate electrode 26 works as an end point detector, and the gate electrode 26 on the thick gate oxide film 24 of the high pressure part 22 is left behind [drawing 5 (f)].

[0011]

[Problem(s) to be Solved by the Invention] Although the thin gate oxide film 23 and the thick gate oxide film 24 can be formed by almost exact thickness by the conventional method of above-mentioned drawing 4 , there is a problem which the defect of the gate pressure-proofing to the circuit element of the integrated circuit device using them and the defect on an operating characteristic generate in the probability which is the grade which cannot be disregarded although many [, of course / seldom]. When the cause is investigated in detail, the still poorer main causes have a defect in the point that the gate oxide film 24 thick in the photo etching process of drawing 4 (c) is polluted with the impurity of a photoresist 19 that it is easy to generate in the direction of the circuit element using the thick gate oxide film 24, and increasing from immediately after manufacture along with progress of a time made the probability of poor generating by this clear.

[0012] Then, selection of a photoresist 19, change of the conditions of the rotation application and heating solidification, selection of ashing conditions or remover liquid, and various meanses, such as thoroughness-izing of post-washing after removal, are taken further, the improvement effect like ** is not accepted in each-other gap, either, but probably, the oxide film which the photoresist 19 contacted will be polluted by impurities, and a ****** short time is also easily considered to be unremovable with the usual means. Although using things other than photoresist 19 as a mask is also considered, since a photograph process is required if it is an object for selective etching at all, use of a photoresist 19 cannot be excluded. Moreover, even if it increases the thickness of the thick gate oxide film 24 further, improvement effects are few and tend to bring a result to which the threshold of the gate of operation exceeds tolerance.

[0013] On the other hand, although according to the method of above-mentioned drawing 5 the gate oxide films 23 and 24 from which thickness differs did not contact a photoresist 19 and it was not polluted with the impurity in a photoresist 19, it generated in the probability of the grade which neither the defect of gate pressure-proofing nor the defect on an operating characteristic can ignore too to the circuit element of the integrated circuit device using them.

[0014] When the cause was investigated in detail, it turns out that it is because a poor cause has an undercut in the thick gate oxide film 24 under the gate electrode 26 of the high pressure part 22. that is, the gate electrode 26 of the high pressure part 22 was formed with photo etching technology at the process of drawing 5 (c) -- the back, although complete etching by fluoric acid is performed before forming the thin gate oxide film 23 of the logic section 21, the gate oxide film 24 with thick portions other than under the gate electrode 26 of the high pressure part 22 is also simultaneously removed at this time And since etching by fluoric acid is isotropic etching, a part for the periphery of the oxide film under the gate electrode 26 of the high pressure part 22 **********s inevitably, and the so-called undercut enters. Then, although the thin oxide film 23 is formed also in an undercut portion, the membraneous quality of the oxide film of a boundary portion is inadequate, and the problem of pressure-proofing of a gate oxide film falling occurs.

[0015] The purpose of this invention is to offer the manufacture method of the MOS type integrated circuit device which has the reliable gate insulator layer without a poor gate proof pressure from which thickness differs in view of the above problems.

[0016]

[Means for Solving the Problem] The selective oxidation process which oxidizes thermally where all the parts that face [forming the gate oxide film from which thickness differs to the wafer for MOS type integrated circuit devices according to this invention] the above-mentioned purpose, and should form a gate oxide film are covered with an oxidation-resistant film, It is attained by the membrane formation method including the first oxidization process which forms the gate oxide film of the thicker one by thermal oxidation where an oxidation-resistant film is left to the part which should attach the gate oxide film of the thinner one, and the

second oxidization process which forms the gate oxide film of the thinner one by thermal oxidation where an oxidation-resistant film is removed.
[0017] It is good for the oxidation-resistant film said to the above-mentioned composition that using the silicon nitride film suitable for attaching an isolation film or a field oxide film at a selective oxidation process attaches a buffer oxide film thin on the surface of a wafer as the ground well. In order to leave this oxidation-resistant film to the part which should attach a thin gate oxide film for the first oxidization process, it is good to remove an oxidation-resistant film from the membrane formation part of a thick gate oxide film by the plasma etching method, where it is covered by mask films, such as a photoresist. In order to remove this oxidation-resistant remaining film for the second oxidization process, it is good to give wet etching using the etching reagent which has selectivity to it, and it is very advantageous to use heat phosphoric acid especially as an etching reagent at the point which raises [rather than] the selectivity of wet etching 100 or more times to a thick gate oxide film.
[0018] In addition, the thermal oxidation for forming each shall depend a thick gate oxide film and a thin gate oxide film on the so-called pie ROJIE nick oxidation style at the first oxidization process and the second oxidization process. the thick gate oxide film which forms membranes at the first oxidization process although it is possible to form a thin gate oxide film by desired thickness simply at the second oxidization process -- the following second oxidization process -- stacking -- increase -- since it generates -- beforehand -- this -- stacking -- increase -- a part -- it is good to attach by thickness thinner than the expected last target thickness furthermore, when preparing a buffer oxide film as a ground of an oxidation-resistant film as mentioned above, in case an oxidation-resistant film is removed for the second oxidization process, the film pressure of a gate oxide film with it also of it is almost the same as that of the thickness of a buffer oxide film -- since it ******, as for the thick gate oxide film by the first oxidization process, it is desirable to attach by the thickness which also expected this decrement beforehand [good removing simultaneously and] [thick in this case]
[0019] moreover, as the another manufacture method of an MOS type semiconductor device of having two gate oxide films from which thickness differs on the same semiconductor substrate The selective oxidation process which oxidizes thermally where all the parts that should form a gate oxide film are covered with an oxidation-resistant film, The process which forms the gate oxide film of one thickness, and the electrode layer which should process a gate electrode in all the parts that should form a gate oxide film, The process which removes the oxide film and electrode layer of all the parts that should form the gate oxide film of another side, The process which forms the gate oxide film of the thickness of another side, and the electrode layer which should process a gate electrode in all the parts that should form a gate oxide film, The method of performing the process which removes the electrode layer of the upper layer of the part in which the electrode layer of a bilayer was formed, and the process which processes a gate electrode from an electrode layer one by one can also be taken.
[0020] The gate oxide film of the thicker one shall be then formed ahead of the gate oxide film of the thinner one. It is good to form a gate oxide film by the pie ROJIE nick oxidation style also in this case.
[0021]
[Function] The membrane formation method of the gate oxide film by this invention still in the state in the state where it was covered with the oxidation-resistant film since all the parts that should form a gate oxide film were selective oxidation processes Perform photo etching surely required in order to distinguish mutually the membrane formation range of a thick gate oxide film and a thin gate oxide film, and it leaves an oxidation-resistant film only to the membrane formation range of a thin gate oxide film. By forming only a thick gate oxide film, after this has covered the membrane formation range of a thin gate oxide film at the first oxidization process, and forming a thin gate oxide film, where this oxidation-resistant remaining film is also removed at the second oxidization process A photograph process is substituted for the state where the membrane formation part is still covered by the oxidation-resistant film, before it also to which oxidization process which forms a gate oxide film. Therefore, a gate oxide film abolishes a possibility that a gate oxide film may be polluted with the impurity, as the photoresist resin containing impurities, such as a metal, of course, cannot contact the wafer side of the membrane formation range, either. And there is no undercut in the gate oxide film under a gate electrode, and the fall of gate pressure-proofing is avoided also at this point.
[0022] Moreover, also in the manufacture method according to above, a gate electrode layer is always between a gate oxide film and a photoresist, and direct contact is avoided. Therefore, a gate oxide film abolishes a possibility that a gate oxide film may be polluted with the impurity, as the photoresist resin containing impurities, such as a metal, of course, cannot contact the wafer side of the membrane formation range, either. And there is no undercut in the gate oxide film under a gate electrode, and the fall of gate pressure-proofing is avoided also at this point.
[0023] In addition, although thermal oxidation can also be based on a dry oxidation style or a steam oxidation style, when being based on the so-called pie ROJIE nick oxidation style gathers the speed of membrane formation and it can raise the control precision of film pressure, it is the most advantageous.
[0024]
[Example] The example of the manufacture method of the semiconductor device of this invention is explained referring to drawing which gave the same sign to drawing 4 , drawing 5 , and the common portion hereafter. Drawing 1 is a cross section for every main processes of the first example concerning the manufacture method of the semiconductor device of this invention. Drawing 1 (a) shows the state of a selective oxidation process. The wafer 10 with which drawing should make an integrated circuit is a part very much, and MOS transistors 41 and 42 the right half and left half of drawing were indicated to be to drawing 2 are the fields made, respectively. In an integrated circuit device, it is an object for the drive of a display panel, and MOS transistor 42 of the high pressure part 22 in the right half of drawing for the pixel drive operates under the voltage of 40-50V, and MOS transistor 41 of the logic section 21 in the left half of drawing which carries out high-speed operation for indicative datas operates

under the voltage of 5V. The gate oxide film of these MOS transistors 41 and 42 is made into the thickness according to this operating voltage, and is set as 25nm and 150nm, respectively in this example as well as drawing 4 and the conventional example of 5.

[0025] The semiconductor regions 11 of a wafer 10 are a semiconductor substrate, an epitaxial layer, and a well, in this example, the buffer oxide film 12 is attached to the front face by thermal oxidation by 35nm thickness, and a silicon nitride film is formed by CVD for the oxidation-resistant films 13 at 150nm thickness. At the selective oxidation process of drawing 1 (a), as shown in drawing, after forming each transistor field in a wrap pattern, the isolation film or the field oxide film 14 which encloses each field like illustration is formed for the oxidation-resistant film 13 by about 600-800nm thickness by giving thermal oxidation by the so-called LOCOS method.

[0026] Drawing 1 (b) is a preparation process for the first oxidization process of drawing 1 (c), leaves the range which should attach the thin gate oxide film in the left half of drawing, and removes the oxidation-resistant film 13 by photo etching. for this reason -- being alike -- it is good for plasma etching to remove the oxidation-resistant film 13 within the controlled atmosphere which contains 3 nitrogen fluoride (NF3) after forming a photoresist 19 in the photograph process using the usual photoresist 19 as a mask, as shown in drawing, and to remove the buffer oxide film 12 of the bottom by easy etching with rare fluoric acid liquid, and to expose the front face of a semiconductor region 11 There is no possibility that a photoresist 19 may be contacted and it may be polluted with the photograph process of the process of this drawing 1 (b) since the front face or the buffer oxide film 12 of a semiconductor region 11 is separated from the photoresist 19 with the oxidation-resistant film 13.

[0027] Following drawing 1 (c) shows the state of the first oxidization process. At this process, where the range in the left half of drawing which should remove a photoresist 19 from the state of front drawing 1 (b) with meanses, such as ashing, first, and should attach a thin gate oxide film is covered by the oxidation-resistant film 13, the front face of the semiconductor region 11 of a right half is oxidized thermally, and the thick gate oxide film 24 is formed. This gate oxide film 24 is advantageous at the point that forming membranes by the so-called pie ROJIE nick oxidation style (PAIRO oxidization being called henceforth) which uses the gas reaction of hydrogen and oxygen like usually can raise membrane formation speed and membraneous quality. In this example, the gate oxide film 24 thick on 900 degrees C and the PAIRO oxidization conditions for about 80 minutes is formed by 170nm thickness thicker than 150nm of desired value.

[0028] At the preparation process for the following second oxidization process shown in drawing 1 (d), the oxidation-resistant film 13 and the buffer oxide film 12 are removed from the range in the left half of drawing. First, if it is good that removal of the oxidation-resistant film 13 is based on the wet etching using the etching reagent which has the highest possible selectivity to the oxidation-resistant film 13 so that the thick gate oxide film 24 may not be affected as much as possible and it uses heat phosphoric acid especially as this etching reagent, about 200:1 high etch selectivity will be obtained to the oxidation-resistant film 13 which consists of a silicon nitride film, and the thick gate oxide film 24. although it is possible for the following buffer oxide film 12 to remove by wet etching with usual rare fluoric acid liquid, since there is no etch selectivity in this case, in case the buffer oxide film 12 of the 35nm above-mentioned thickness is removed, the thick gate oxide film 24 is the same -- ** etching is carried out and thickness decreases from 170nm to 135nm In addition, in process in this drawing 1 (d), although the thick gate oxide film 24 contacts heat phosphoric acid and rare fluoric acid, there are very few possibilities that contact to these inorganic acids may receive contamination, as everyone knows.

[0029] At the second oxidization process of following drawing 1 (e), the clean surface of the semiconductor region 11 of the left half which removed the oxidation-resistant film 13 and the buffer oxide film 12, and was exposed at the last process is oxidized thermally, and the thin gate oxide film 23 is attached. It is good to use a PAIRO oxidation style also for this thermal oxidation, for example, it forms the thin gate oxide film 23 to the 25nm thickness of desired value under 800 degrees C and the conditions which are about 40 minutes. Since the growth rate of an oxide film falls as thickness increases, although the thick gate oxide film 24 is also stacked and increases simultaneously with this, from growth of the thin gate oxide film 23, about 15nm of lows stacks and increases, and they become the thickness near the desired value of 150nm from 135nm of a last process. Then, the polycrystal silicon film 15 accumulates by reduced pressure CVD.

[0030] Furthermore, in this drawing (f), it is applied, patterning of the photoresist 19 is carried out, and the gate electrode 25 of the logic section 21 and the gate electrode 26 of the high pressure part 22 are formed of the photo etching of the polycrystal silicon film 15. Although even membrane formation of the gate oxide films 23 and 24 by this invention method and formation of the gate electrodes 25 and 26 are completed above Since photo etching is substituted for the state where the oxidation-resistant film 13 of drawing 1 (a) before the first oxidization process of drawing 1 (c) and the second oxidization process of drawing 1 (e) is still shown in the front face of a wafer 10, at the preparation process of drawing 1 (b) Since the front face of the semiconductor region 11 of the range which should form them is not contacted as well as the ability of a photoresist 19 not to contact the gate oxide film 23 or 24, either, the gate oxide films 23 and 24 which do not have contamination by the impurity in a pure semiconductor front face can be easily formed by good membraneous quality.

[0031] The cross section in a next process is shown in drawing 2 (a) and (b) simple for reference. In drawing 2 (a), the gate electrodes 25 and 26 and the field oxide film 14 are used as a mask, or n type low concentration field 32 is diffused for MOS transistors 42 of the high pressure part 22 on the front face of the p type semiconductor region 11 with the mask by photo etching technology, and n type source field 33 and n type drain field 34, and p type contact field 35 are diffused to MOS transistors 41 and 42 of the logic section 21 and the high pressure part 22. This process can be performed with the gate oxide films 23 and 24 left.

[0032] Finally ****** is made the oxide film of the key point, the electrode 36 of an aluminium alloy is arranged, and the source terminal S, the drain terminal D, and gate-terminal G are derived [drawing 2 (b)]. Thus, operating voltage can make mutually

different MOS transistors 41 and 42 as an example of the circuit element of an integrated circuit to a wafer 10. In addition, although a layer insulation film is prepared on the gate electrodes 25 and 26 and a protective coat is prepared in fact on an electrode 36, respectively, it is omitted drawing.

[0033] In the test result of the integrated circuit device which included MOS transistors 41 and 42 in the wafer 10 which formed the gate oxide films 23 and 24 by this invention method like drawing 2 As opposed to the defect of gate pressure-proofing or a threshold by whom contamination is considered to be the cause having occurred according to 1 - 3% of probability in the former When based on this invention method, the poor probability of occurrence which starts immediately after manufacture is about 0, and neither gate pressure-proofing nor especially degradation of an operating characteristic was further accepted also by the result of the degradation accelerated test of about 100 hours under heating.

[0034] Drawing 3 (a) or (f) is a cross section for every main processes of the example of the another manufacture method of this invention. Drawing 3 (a) shows the state of a selective oxidation process like drawing 1 (a). The wafer 10 with which drawing should make an integrated circuit is a part very much, and MOS transistors 41 and 42 the right half and left half of drawing were indicated to be to drawing 2 are the fields made, respectively.

[0035] The semiconductor regions 11 of a wafer 10 are a semiconductor substrate, an epitaxial layer, and a well, in this example, the buffer oxide film 12 is attached to the front face by thermal oxidation by 35nm thickness, and a silicon nitride film is formed by the plasma CVD method as an oxidation-resistant film 13 at 150nm thickness. At the selective oxidation process of drawing 3 (a), as shown in drawing, after forming each transistor field in a wrap pattern, the isolation film or the field oxide film 14 which encloses each field like illustration is formed for the oxidation-resistant film 13 by about 600-800nm thickness by giving thermal oxidation by the so-called LOCOS method.

[0036] After removing the oxidation-resistant film 13 and the buffer oxide film 14, the first polycrystal silicon film 15 is continuously formed the 150nm thick oxide film 24 for the high pressure parts 22 and deposited on the whole surface by reduced pressure CVD by 900 degrees C and PAIRO oxidization for about 61 minutes, a photoresist 19 is applied, and pattern formation is carried out on the high pressure part 22 [drawing 3 (b)]. Next, after carrying out etching removal of the first polycrystal silicon film 15 on the logic section 21, a photoresist 19 is removed, the thick gate oxide film 26 on the logic section 21 is **********ed by fluoric acid, and the front face of a semiconductor region 11 is exposed [drawing 3 (c)]. Since the high pressure-part 22 top has the polycrystal silicon film 15, the gate oxide film 24 does not **********. And since the first polycrystal silicon film 15 on the high pressure part 22 remains more greatly than the active region of the high pressure part 22 if it puts in another way, since the first polycrystal silicon film 15 on the high pressure part 22 remains so that the high pressure-part 22 whole may be covered, the undercut of the oxide film [directly under] of the gate electrode 26 formed of photo etching later does not happen.

[0037] After an appropriate time, the second gate oxide film 23 is formed in thickness of 25nm by 800 degrees C and PAIRO oxidization for about 40 minutes. At this time, the first polycrystal silicon film 15 of the high pressure part 22 also oxidizes, and an oxide film 18 is formed on it. Then, the second polycrystal silicon film 16 is deposited on the whole surface, a photoresist 19 is applied, and pattern formation is carried out on the logic section 21 [drawing 3 (d)].

[0038] Next, etching removal of the second polycrystal silicon film 16 of the high pressure part 22 is carried out. Since the oxide film 18 on the first polycrystal silicon film 15 of the high pressure part 22 described previously works as an end point detector of this etching at this time, the first polycrystal silicon film 15 of the high pressure part 22 does not **********. If a photoresist 19 is removed and there is need, the oxide film 18 on the first polycrystal silicon film 15 can also be **********ed at this time [drawing 3 (e)]. In this state, the second polycrystal silicon film 16 exists in the high pressure part 22 in the state where the first polycrystal silicon film 15 is raw again at the logic section 21. If there is need, the impurity for forming the polycrystal silicon films 15 and 16 into low resistance will be introduced. However, this process is oak needlessness used as the so-called doped polycrystal silicon film which introduces an impurity simultaneously, when depositing a polycrystal silicon film.

[0039] Subsequently, pattern formation of the photoresist 19 is applied and carried out, and the gate electrode 25 of the logic section 21 and the gate electrode 26 of the high pressure part 22 are formed [drawing 3 (f)]. Although even membrane formation of the gate oxide films 23 and 24 by this invention method and formation of the gate electrodes 25 and 26 are completed above, by the above method, in drawing 3 (c) of the process which uses a photoresist 19, and (e), the polycrystal silicon films 15 and 16 are always under a photoresist 19, a photoresist 19 touches the gate oxide films 23 and 24, and impurity contamination is not caused, either. The gate oxide films 23 and 24 which do not have contamination by the impurity in a pure semiconductor front face can be easily formed by good membraneous quality. Moreover, the undercut of the gate oxide film under the gate electrodes 25 and 26 is not carried out.

[0040] The process after this is the same as what was shown with the cross section to drawing 2 (a) and (b), and good for them. At the test result of the integrated circuit device which included MOS transistors 41 and 42 in the wafer 10 which formed the gate oxide films 23 and 24 by this invention method like drawing 2 , the defect of gate pressure-proofing or a threshold by whom the undercut of the oxide film under contamination or a gate electrode is considered to be the cause is about 0, and neither gate pressure-proofing nor especially degradation of an operating characteristic was further accepted also by the result of the degradation accelerated test of about 100 hours under heating.

[0041] In the above-mentioned example, the thick gate oxide film 24 was formed previously, and [drawing 3 (b)] and the gate oxide film 23 thin after that were formed [drawing 3 (d)]. Although this can be made reverse, the thin gate oxide film 23 can be formed first and the thick gate oxide film 24 can also be formed later, it is [at the time of next oxidization] more advantageous to form the thick gate oxide film 24 previously, if loss of weight of the polycrystal silicon film 15 of an eye is further taken into consideration.

[0042] In addition, although thermal oxidation can also be based on a dry oxidation style or a steam oxidation style, when being based on the so-called pie ROJIE nick oxidation style gathers the speed of membrane formation and it can raise the control precision of film pressure, it is the most advantageous.
[0043]
[Effect of the Invention] As explained above, in order to form the gate oxide film from which thickness differs in this invention primary method to the wafer which should incorporate an integrated circuit, Where an oxidation-resistant film is covered in all the parts that should form a gate oxide film in a selective oxidation process first, it oxidizes thermally to a wafer. Where this oxidation-resistant film is left to the membrane formation part of a thin gate oxide film, at the first oxidization process, a thick gate oxide film is formed by thermal oxidation. Where all oxidation-resistant films are furthermore removed at the second oxidization process, a thin gate oxide film is formed by thermal oxidation. by the second method of this invention The gate oxide film of one thickness and the electrode layer which should process a gate electrode are formed in all the parts that should form a gate oxide film. The oxide film and electrode layer of all parts which should form the gate oxide film of another side are removed. The following effect is acquired by removing the electrode layer of the upper layer of the part in which the gate oxide film of the thickness of another side and the electrode layer which should process a gate electrode were formed in all the parts that should form a gate oxide film, and the electrode layer of a bilayer was formed.
[0044] (a) The photograph process using a photoresist in the state where the membrane formation part of a gate oxide film is still covered by the oxidation-resistant film in the primary method Since a gate oxide film, of course, cannot contact the wafer side of the membrane formation range, either, the photoresist resin with which detrimental impurities, such as a metal, are easy to be contained since the second method is managed in the state where it is covered by the electrode layer The gate oxide film which is not polluted by the front face of the pure semiconductor of a wafer with an impurity can be formed easily [in good membraneous quality] and certainly.
[0045] (b) Since the gate oxide film directly under a gate electrode is not exposed to fluoric acid and there is also no undercut directly under a gate electrode, don't reduce the reliability of a device. It sets especially to a primary method (c). An above-mentioned effect is acquired with the same number of processes as the former. That is, since a thin gate oxide film is formed for a thick gate oxide film by the second oxidization process at the first oxidization process, respectively after performing photo etching at the preparation process after a selective oxidation process with this invention method to having inserted the photo etching process between the membrane formation process of a thick gate oxide film, and the membrane formation process of a thin gate oxide film conventionally, it is the same at the point which goes via the oxidization process of two times, and 1 time of a photo etching process. In addition, as everyone knows, since a selective oxidation process is a process general to every integrated circuit, it is not necessary to add it especially for this invention. And the embodiment of this invention which removes an oxidation-resistant film from the membrane formation part of a thick gate oxide film by the plasma etching method for a start for an oxidization process has the advantage which a possibility that a photoresist film may receive an injury is decreased and makes photo etching easier than the wet etching method. Moreover, the mode which removes an oxidation-resistant film from the membrane formation part of a thin gate oxide film by wet etching using the etching reagent which has selectivity to it, especially heat phosphoric acid liquid for the second oxidization process has the effect of decreasing the influence which it has on a thick gate oxide film, and giving it exact thickness.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The manufacture method of the MOS type integrated circuit device which has two gate oxide films which are characterized by providing the following, and from which thickness differs on the same semiconductor substrate The selective oxidation process which oxidizes thermally where all the parts that should form a gate oxide film are covered with an oxidation-resistant film The first oxidization process which forms the gate oxide film of the thicker one by thermal oxidation where an oxidation-resistant film is left to the part which should attach the gate oxide film of the thinner one The second oxidization process which forms the gate oxide film of the thinner one by thermal oxidation where an oxidation-resistant film is removed
[Claim 2] The manufacture method of the MOS type integrated circuit device according to claim 1 characterized by removing the oxidation-resistant film of the membrane formation part of the gate oxide film of the thicker one by the plasma etching method where the oxidation-resistant film of the membrane formation part of the gate oxide film of the thinner one is covered by the mask film.
[Claim 3] The manufacture method of the MOS type integrated circuit device according to claim 1 or 2 characterized by forming a thick gate oxide film at the first oxidization process by the thickness in the second oxidization process which stacked, increased and expected the part.
[Claim 4] The manufacture method of the MOS type integrated circuit device according to claim 3 characterized by making it form membranes by the thickness which expected the decrement at the time of removing both an oxidation-resistant film and the buffer oxide film of the bottom for a thick gate oxide film at the first oxidization process for the second oxidization process.
[Claim 5] The manufacture method of the MOS type integrated circuit device according to claim 1 to 4 characterized by removing an oxidation-resistant film using the etching reagent which has selectivity to it at the second oxidization process.
[Claim 6] The manufacture method of the MOS type integrated circuit device according to claim 5 characterized by using heat phosphoric acid as an etching reagent of selectivity.
[Claim 7] In the manufacture method of the MOS type integrated circuit device which has two gate oxide films from which thickness differs on the same semiconductor substrate The selective oxidation process which oxidizes thermally where all the parts that should form a gate oxide film are covered with an oxidation-resistant film, The process which forms the gate oxide film of one thickness, and the gate electrode layer which should process a gate electrode in all the parts that should form a gate oxide film, The process which removes the oxide film and gate electrode layer of all the parts that should form the gate oxide film of another side, The process which forms the gate oxide film of the thickness of another side, and the gate electrode layer which should process a gate electrode in all the parts that should form a gate oxide film, The manufacture method of the MOS type integrated circuit device characterized by performing the process which removes the gate electrode layer of the upper layer of the part in which the gate electrode layer of a bilayer was formed, and the process which processes a gate electrode from a gate electrode layer one by one.
[Claim 8] The manufacture method of the MOS type integrated circuit device according to claim 7 characterized by forming a gate oxide film with thicker thickness previously, and forming the gate oxide film of the thinner one later.
[Claim 9] The manufacture method of the MOS type integrated circuit device according to claim 1 to 8 characterized by forming a gate oxide film by the pie ROJIE nick oxidation style.

[Translation done.]

PAT-NO: JP408130250A
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TITLE: FABRICATION OF MOS TYPE INTEGRATED CIRCUIT DEVICE
PUBN-DATE: May 21, 1996

INVENTOR-INFORMATION:

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ASSIGNEE-INFORMATION:

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FUJI ELECTRIC CO LTD	N/A

APPL-NO: JP07043723
APPL-DATE: March 3, 1995

INT-CL (IPC): H01L021/8234 , H01L027/088 , H01L029/78 , H01L021/336

ABSTRACT:

PURPOSE: To deposit gate oxides with different thickness on the wafer of an integrated circuit device while protecting the wafer against contamination with a photoresist resin during photoprocess.

CONSTITUTION: Under a state where the part for depositing gate oxides 23, 24 on the surface of a wafer 10 is covered entirely with an anti-oxidation film 13, e.g. silicon nitride, a field oxide 14 is provided through selective oxidation. The anti-oxidation film 13 is then removed from the part for depositing the gate oxide 24 by photoetching. In other words, a thick gate oxide 24 is deposited by thermal oxidation while covering the part for deposition the thin gate oxide 23 with the anti-oxidation film 13. Furthermore, under a state where the anti- oxidation film 13 is removed entirely from the surface of the wafer 10, the thin gate oxide 23 is deposited by thermal oxidation and then the thick gate oxide 24 is deposited thereon. Consequently, the gate oxides 23, 24 having different thickness are deposited for the transistors 41, 42 at a logic part 21 and a high breakdown strength part 22.

DERWENT-ACC-NO: 1996-297961

DERWENT-WEEK: 199630

TITLE: MOS type integrated circuit device mfr. with reduced resin pollution - including removal of thin gate oxide film from wafer by heat oxidn. process

PATENT-ASSIGNEE: FUJI ELECTRIC CO LTD[FJIE]

PRIORITY-DATA: 1994JP-0210326 (September 5, 1994)

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ABSTRACTED-PUB-NO: JP 08130250A

BASIC-ABSTRACT:

Mfr. involves performing selection oxidn. process on a field oxide film (14) which is formed on a wafer (10). An oxidn.-resistant film (13) such as silicon nitride film is formed over the wafer. The oxidn.-resistant film is removed at predetermined portions to form a thick gate oxide film (24). By heat oxidn. of the thick gate oxide film, a thin gate oxide film (23) is formed. The thin gate oxide film is then removed from the wafer thereby increasing the size of the thick gate oxide film. A 1st transistor of a logic part (21) and a 2nd transistor of a high breakdown voltage part (22) with differing thickness is formed on the gate oxide film.

ADVANTAGE - Avoids pollution by resin at time of photoprocessing. Reduces influence due to thick gate oxide film.

CHOSEN-DRAWING: Dwg.1/5

DERWENT-CLASS: L03 U11 U12

CPI-CODES: L04-C07; L04-C12A; L04-C12B; L04-E01B;

EPI-CODES: U11-C05B1; U11-C05F1; U11-C18A3; U12-D02;

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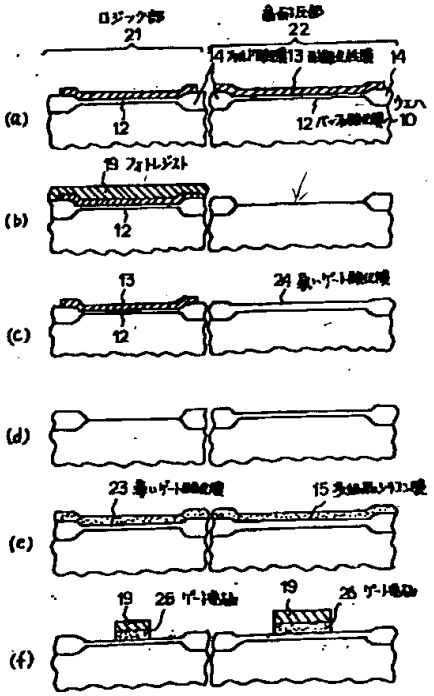
(54)【発明の名称】　ＭＯＳ型集積回路装置の製造方法

(57)【要約】

【目的】集積回路装置のウェハに膜厚が互いに異なるゲート酸化膜をフォトプロセス時にフォトレジスト用の樹脂で汚染されることなく成膜する。

【構成】ウェハ１０の表面のゲート酸化膜２３や２４を成膜すべき全ての個所を窒化シリコン等の耐酸化性膜１３で覆った状態でフィールド酸化膜１４を付ける選択酸化を施した後にフォトエッチングを施して、耐酸化性膜１３を厚いゲート酸化膜２４を成膜すべき個所から除去し、従って薄いゲート酸化膜２３の成膜個所に耐酸化性膜１３を被覆した状態で熱酸化によって厚いゲート酸化膜２４を成膜し、さらにウェハ１０の表面から耐酸化性膜１３をすべて除去した状態で熱酸化によって薄いゲート酸化膜２３を成膜しかつ厚いゲート酸化膜２４を積み増すことにより、ロジツク部２１および高耐圧部２２のトランジスタ４１と４２用に膜厚が互いに異なるゲート酸化膜２３と２４を成膜する。



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【特許請求の範囲】

【請求項1】同一半導体基板上に厚さの異なる二つのゲート酸化膜を有するMOS型集積回路装置の製造方法において、ゲート酸化膜を成膜すべきすべての個所を耐酸化性膜により覆った状態で熱酸化を施す選択酸化工程と、薄い方のゲート酸化膜を付けるべき個所に耐酸化性膜を残した状態で熱酸化により厚い方のゲート酸化膜を成膜する第一酸化工程と、耐酸化性膜を除去した状態で熱酸化により薄い方のゲート酸化膜を成膜する第二酸化工程とを含むことを特徴とするMOS型集積回路装置の製造方法。

【請求項2】薄い方のゲート酸化膜の成膜個所の耐酸化性膜をマスク膜で覆った状態で厚い方のゲート酸化膜の成膜個所の耐酸化性膜をプラズマエッチング法により除去するようにしたことを特徴とする請求項1に記載のMOS型集積回路装置の製造方法。

【請求項3】第一酸化工程では厚いゲート酸化膜を第二酸化工程における積み増し分を見込んだ膜厚で成膜するようにしたことを特徴とする請求項1または2に記載のMOS型集積回路装置の製造方法。

【請求項4】第一酸化工程では厚いゲート酸化膜を第二酸化工程のために耐酸化性膜とその下側のバッファ酸化膜をともに除去する際の減少分を見込んだ膜厚で成膜するようにしたことを特徴とする請求項3に記載のMOS型集積回路装置の製造方法。

【請求項5】第二酸化工程で耐酸化性膜をそれに対し選択性をもつエッチング液を用いて除去するようにしたことを特徴とする請求項1ないし4のいずれかに記載のMOS型集積回路装置の製造方法。

【請求項6】選択性のエッチング液として熱燐酸を用いることを特徴とする請求項5に記載のMOS型集積回路装置の製造方法。

【請求項7】同一半導体基板上に厚さの異なる二つのゲート酸化膜を有するMOS型集積回路装置の製造方法において、ゲート酸化膜を成膜すべきすべての個所を耐酸化性膜により覆った状態で熱酸化を施す選択酸化工程と、ゲート酸化膜を成膜すべきすべての個所に一方の膜厚のゲート酸化膜とゲート電極を加工すべきゲート電極膜とを形成する工程と、他方のゲート酸化膜を成膜すべきすべての個所の酸化膜とゲート電極膜を除去する工程と、ゲート酸化膜を成膜すべきすべての個所に他方の膜厚のゲート酸化膜とゲート電極を加工すべきゲート電極膜とを形成する工程と、二層のゲート電極膜が形成された個所の上層のゲート電極膜を除去する工程と、ゲート電極膜からゲート電極を加工する工程とを順次行うことを特徴とするMOS型集積回路装置の製造方法。

【請求項8】膜厚の厚い方のゲート酸化膜を先に形成し、薄い方のゲート酸化膜を後から成膜することを特徴とする請求項7に記載のMOS型集積回路装置の製造方法。

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【請求項9】ゲート酸化膜をパイロジェニック酸化法により成膜するようにしたことを特徴とする請求項1ないし8のいずれかに記載のMOS型集積回路装置の製造方法。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は、動作電圧の互いに異なるMOS型半導体素子、特に互いに膜厚の異なるゲート酸化膜を有するMOS型半導体素子を一個の半導体チップに集積したMOS型集積回路装置の製造方法に関する。

【0002】

【従来の技術】集積回路装置の用途の拡大に伴って、同一チップ内に負荷の駆動を目的とした比較的高耐圧、大容量の回路要素と高速動作に適した小容量の回路要素とを作成する技術が重要となってきている。かかる集積回路装置では、負荷駆動用の回路要素（以下この回路要素を高耐圧部と称する）はふつう40～60Vの電源電圧下で、また高速動作用の回路要素（以下この回路要素をロジツク部と称する）はふつう5Vの低圧の制御電源電圧下で動作するので、各回路要素にはその動作電圧に応じた耐圧を与える必要があり、回路要素が絶縁ゲート制御型の素子の場合はそのゲート酸化膜にかかる必要耐圧に応じた膜厚をもたせる必要がある。例えば、ロジツク部の高速動作を可能にするためロジック部のゲート酸化膜の厚さは25～40nmであるが、高耐圧部に関しては40～60Vの電圧がゲート酸化膜にも印加されるため高耐圧部のゲート酸化膜は、130～150nmの厚さが必要である。従ってそのような集積回路装置用のウェハには、膜厚が互いに異なる二種類のゲート酸化膜を成膜することが必要である。

【0003】図4は、そのような集積回路装置用のウェハの膜厚が互いに異なる二種類のゲート酸化膜上にゲート電極を形成するまでの従来方法を、主な工程ごとの断面図で示す。図4（a）において、ウェハ10の半導体領域11は半導体基板やエピタキシャル層やウェルである。従来の選択酸化技術により、ウェハ10の一方の主面に素子分離のためのフィールド酸化膜14が半導体素子を作り込むべき各範囲を取り囲むように形成された状態の断面図である。12はバッファ酸化膜、13は例えば窒化シリコン膜のような耐酸化性膜である。図の左側はロジック部21で薄いゲート酸化膜を、右側は高耐圧部22で厚いゲート酸化膜をそれぞれ成膜すべき部分である。

【0004】次に、耐酸化性膜13とバッファ酸化膜12を除去した後、（薄いゲート酸化膜を成膜すべき図の左側の範囲を含む）ウェハ10の全面に、900℃、57分程度のパイロ酸化により厚いゲート酸化膜24をまず成膜する〔図4（b）〕。高耐圧部のゲート酸化膜24の最終膜厚を150nm程度としたいとき、この工程

では薄めの例えば１３５ｎｍの膜厚に成膜する。

【０００５】続いて、図の右側の高耐圧部２２をフォトレジスト１９で覆い、例えば希ふっ酸を用いるウェットエッチングで、フォトレジスト１９で覆われていない図の左側のロジツク部２１の厚い酸化膜２４を除去し、半導体領域１１の表面を露出させる〔図４（ｃ）〕。さらに、アッシングやリムーバ液によってウェハ１０の表面からフォトレジスト１９を除去した後、８００℃、４０分程度のパイロ酸化を行う。これにより、ロジック部２１には厚さ２５ｎｍ程度の薄いゲート酸化膜２３が成膜される。また、これと同時に図の右側の高耐圧部２２も熱酸化されるので厚いゲート酸化膜２４が積み増されるが、熱酸化時の酸化膜の成長速度は膜厚の増加とともに低下するから厚いゲート酸化膜２４は例えば１５ｎｍだけ積み増されて目標の１５０ｎｍにほぼ等しい膜厚になる〔図４（ｄ）〕。ここでゲート酸化膜の成長速度がロジック部２１と高耐圧部２２で異なるのは、酸化反応が酸化膜とシリコン基板との界面において、酸化膜中を拡散してきた酸化種によって進行するためである。そのため酸化膜が厚くなるに従って酸化種が酸化膜とシリコン基板との界面に到達するのが困難になり、成長速度が遅くなるのである。

【０００６】その後、減圧ＣＶＤ法により、ウェハ１０の全面に多結晶シリコン膜１５を堆積する〔図４（ｅ）〕。更に、フォトエッチング技術により、薄いゲート酸化膜２３上にロジック部のゲート電極２５を、また厚いゲート酸化膜２４上高耐圧部のゲート電極２６を形成する〔図４（ｆ）〕。

【０００７】図５は、集積回路装置用のウェハの膜厚が互いに異なる二種類のゲート酸化膜上にゲート電極を形成するまでの別の方法を主な工程ごとの断面図で示す。図５（ａ）は、図４（ａ）と同じく選択酸化技術により、ウェハ１０の一方の主面に素子分離のためのフィールド酸化膜１４が半導体素子を作り込むべき各領域を取り囲むように形成された状態の断面図である。１２はバッファ酸化膜、１３は例えば窒化シリコン膜のような耐酸化性膜である。図の左側はロジック部２１で薄いゲート酸化膜を、右側は高耐圧部２２で厚いゲート酸化膜をそれぞれ成膜すべき部分である。

【０００８】まず、耐酸化性膜１３とバッファ酸化膜１２を除去した後、ウェハ１０の全面に、９００℃、６１分程度のパイロ酸化により厚さ１５０ｎｍの厚いゲート酸化膜２４を成膜し、続いて減圧ＣＶＤ法により、第一の多結晶シリコン膜１５をウェハ１１の全面に堆積する〔図５（ｂ）〕。次に、フォトレジスト１９を塗布し、パターン形成して高耐圧部２２のゲート電極２６を形成する〔図５（ｃ）〕。

【０００９】さらに、アッシングやリムーバ液によってウェハ１０の表面からフォトレジスト１９を除去した後、ふっ酸による全面エッチングを行うと、ロジック部

２１の厚いゲート酸化膜２４は除去され、半導体領域１１の表面が露出するが、高耐圧部２２においては、ゲート電極２６の下の厚い酸化膜２４はエッチングされないで残る〔図５（ｄ）〕。

【００１０】しかる後に第二のゲート酸化を、８００℃、４０分程度行い、ロジック部２１の薄いゲート酸化膜２３を２５ｎｍ程度成膜する。このとき高耐圧部２２のゲート電極２６も酸化され、ゲート電極２６の上に酸化膜１８が形成される。続いて第二の多結晶シリコン膜１６を全面に堆積する〔図５（ｅ）〕。更に、フォトレジスト１９を塗布し、フォトエッチング技術により、ロジック部２１の薄いゲート酸化膜２３上にロジック部のゲート電極２５を形成する。同時に高耐圧部２２上の第二の多結晶シリコン膜１６をエッチング除去する。このとき、ゲート電極２６の上の酸化膜１８がエンドポイントディテクタとして働き、高耐圧部２２の厚いゲート酸化膜２４上のゲート電極２６は残される〔図５（ｆ）〕。

【００１１】

【発明が解決しようとする課題】上記図４の従来方法によって、薄いゲート酸化膜２３と厚いゲート酸化膜２４とをほぼ正確な膜厚で成膜できるが、それらを用いた集積回路装置の回路要素にゲート耐圧の不良や動作特性上の不良が、もちろんあまり多くはないが無視できない程度の確率で発生する問題がある。その原因を詳しく調査したところ不良は厚いゲート酸化膜２４を用いた回路要素の方に発生しやすく、更に不良のおもな原因は図４（ｃ）のフォトエツチング工程中に厚いゲート酸化膜２４がフォトレジスト１９の不純物により汚染される点にあり、これによる不良発生の確率は製造直後よりも使用時間の経過につれて増加することが判明した。

【００１２】そこで、フォトレジスト１９の選択、その回転塗布や加熱固化の条件の変更、アッシング条件やリムーバ液の選定、更に除去後の後洗浄の徹底化等の種々の手段を採ってみたがいずれにもさほどの改善効果は認められず、おそらくは例え短時間でもフォトレジスト１９が接触した酸化膜は不純物で汚染されてしまい、通常の手段では容易に除去できないものと考えられる。マスクとしてフォトレジスト１９以外のものを用いることも考えられるが、それが選択エッチング用である以上はフォトプロセスが必要なのでフォトレジスト１９の使用は省けない。また、厚いゲート酸化膜２４の膜厚をさらに増してみても改善効果は僅かであり、かつゲートの動作しきい値が許容限界を越えてしまう結果となりやすい。

【００１３】一方、上記図５の方法によれば、膜厚の異なるゲート酸化膜２３、２４がフォトレジスト１９と接触することはなく、フォトレジスト１９中の不純物によって汚染されることはないはずであるが、それらを用いた集積回路装置の回路要素にゲート耐圧の不良や動作特性上の不良が、やはり無視できない程度の確率で発生し

た。

【0014】その原因を詳しく調査したところ不良原因は、高耐圧部22のゲート電極26下の厚いゲート酸化膜24にアンダーカットがあるためであることがわかった。すなわち、図5（c）の工程で高耐圧部22のゲート電極26をフォトエッチング技術により形成した後、ロジック部21の薄いゲート酸化膜23を成膜する前に、ふっ酸による全面エッチングを行うが、このとき同時に高耐圧部22のゲート電極26の下以外の部分の厚いゲート酸化膜24も除去される。そして、ふっ酸によるエッチングは等方性エッチングであるから必然的に高耐圧部22のゲート電極26の下の酸化膜の周辺部分がエッチングされ、いわゆるアンダーカットが入る。その後、アンダーカット部分にも薄い酸化膜23が形成されるが、境界部分の酸化膜の膜質が不十分で、ゲート酸化膜の耐圧が低下する等の問題が起きるのである。

【0015】本発明の目的は、以上のような問題に鑑み、ゲート耐圧不良等の無い、信頼性の高い、膜厚が異なるゲート絶縁膜を有するMOS型集積回路装置の製造方法を提供することにある。

【0016】

【課題を解決するための手段】上記の目的は本発明によれば、MOS型集積回路装置用のウェハに膜厚が異なるゲート酸化膜を成膜するに際し、ゲート酸化膜を成膜すべき個所をすべて耐酸化性膜により覆った状態で熱酸化を施す選択酸化工程と、薄い方のゲート酸化膜を付けるべき個所に耐酸化性膜を残した状態で熱酸化により厚い方のゲート酸化膜を成膜する第一酸化工程と、耐酸化性膜を除去した状態で熱酸化により薄い方のゲート酸化膜を成膜する第二酸化工程とを含む成膜方法によって達成される。

【0017】上記の構成にいう耐酸化性膜には選択酸化工程で素子分離膜ないしフィールド酸化膜を付けるに適する窒化シリコン膜を用いるのがよく、かつその下地としてウェハの表面に薄いバッファ酸化膜をつけておくのがよい。第一酸化工程のためこの耐酸化性膜を薄いゲート酸化膜を付けるべき個所に残すには、それをフォトレジスト等のマスク膜で覆った状態でプラズマエッチング法によって厚いゲート酸化膜の成膜個所から耐酸化性膜を除去するのがよい。この残った耐酸化性膜を第二酸化工程のために除去するには、それに対して選択性をもつエッチング液を用いてウェットエッチングを施すのがよく、特にエッチング液として熱燐酸を用いるのがウェットエッチングの選択性を厚いゲート酸化膜に対するより100倍以上高める点で非常に有利である。

【0018】なお、第一酸化工程と第二酸化工程で厚いゲート酸化膜と薄いゲート酸化膜をそれぞれを成膜するための熱酸化はいわゆるパイロジェニック酸化法によるものとする。第二酸化工程では薄いゲート酸化膜を単純に所望の膜厚で成膜することでよいが、第一酸化工程で成膜する厚いゲート酸化膜は次の第二酸化工程で積み増しが発生するため、あらかじめこの積み増し分を見込んだ最終の目標膜厚より薄めの膜厚で付けておくのがよい。さらに、前述のように耐酸化性膜の下地としてバッファ酸化膜を設ける場合は、第二酸化工程のため耐酸化性膜を除去する際にそれも同時に除去するのがよく、この際に厚いゲート酸化膜の膜圧がバッファ酸化膜の膜厚とほぼ同じだけ減少するので、第一酸化工程による厚いゲート酸化膜はあらかじめこの減少分も見込んだ膜厚で付けておくのが望ましい。

【0019】また、同一半導体基板上に厚さの異なる二つのゲート酸化膜を有するMOS型半導体装置の別の製造方法として、ゲート酸化膜を成膜すべきすべての個所を耐酸化性膜により覆った状態で熱酸化を施す選択酸化工程と、ゲート酸化膜を成膜すべきすべての個所に一方の膜厚のゲート酸化膜とゲート電極を加工すべき電極膜とを形成する工程と、他方のゲート酸化膜を成膜すべきすべての個所の酸化膜と電極膜を除去する工程と、ゲート酸化膜を成膜すべきすべての個所に他方の膜厚のゲート酸化膜とゲート電極を加工すべき電極膜とを形成する工程と、二層の電極膜が形成された個所の上層の電極膜を除去する工程と、電極膜からゲート電極を加工する工程とを順次行う方法をとることもできる。

【0020】そのとき、厚い方のゲート酸化膜を薄い方のゲート酸化膜より先に形成するものとする。この場合もゲート酸化膜をパイロジェニック酸化法により成膜するのがよい。

【0021】

【作用】本発明によるゲート酸化膜の成膜方法は、ゲート酸化膜を成膜すべき全ての個所が選択酸化工程のため耐酸化性膜により覆われた状態のままで、厚いゲート酸化膜と薄いゲート酸化膜の成膜範囲を互いに区別するために是非必要なフォトエツチングを施して薄いゲート酸化膜の成膜範囲にのみ耐酸化性膜を残し、第一酸化工程ではこれにより薄いゲート酸化膜の成膜範囲を覆った状態で厚いゲート酸化膜だけを成膜し、第二酸化工程ではこの残った耐酸化性膜も除去した状態で薄いゲート酸化膜を成膜することにより、ゲート酸化膜を成膜するいずれの酸化工程に対してもその前にフォトプロセスを成膜個所がまだ耐酸化性膜で覆われている状態で済ませてしまい、従って金属等の不純物を含むフォトレジスト樹脂がゲート酸化膜はもちろんその成膜範囲のウェハ面にも接触し得ないようにして、その不純物によりゲート酸化膜が汚染されるおそれをなくしたものである。しかもゲート電極の下のゲート酸化膜にアンダーカットが無く、この点でもゲート耐圧の低下が避けられる。

【0022】また、上記別の製造方法においても、ゲート酸化膜とフォトレジストとの間にはつねにゲート電極膜があって、直接の接触は避けられている。従って金属等の不純物を含むフォトレジスト樹脂がゲート酸化膜は

もちろんその成膜範囲のウェハ面にも接触し得ないようにして、その不純物によりゲート酸化膜が汚染されるおそれをなくしたものである。しかもゲート電極の下のゲート酸化膜にアンダーカットが無く、この点でもゲート耐圧の低下が避けられる。

【００２３】なお、熱酸化はドライ酸化法やスチーム酸化法によることもできるが、いわゆるパイロジェニック酸化法によるのが成膜の速度を上げ膜圧の制御精度を高め得る上で最も有利である。

【００２４】

【実施例】以下、図４、図５と共通の部分に同一の符号を付した図を参照しながら本発明の半導体装置の製造方法の実施例を説明する。図１は本発明の半導体装置の製造方法に係る第一の実施例の主な工程ごとの断面図である。図１（ａ）は選択酸化工程の状態を示す。図は集積回路を作り込むべきウェハ１０のごく一部であり、図の右半分と左半分が図２に示されたＭＯＳトランジスタ４１と４２がそれぞれ作り込まれる領域である。集積回路装置は例えば表示パネルの駆動用であり、その画素駆動用の図の右半分の高耐圧部２２のＭＯＳトランジスタ４２は４０～５０Ｖの電圧下で動作し、表示データ用の高速動作する図の左半分のロジック部２１のＭＯＳトランジスタ４１は５Ｖの電圧下で動作する。これらのＭＯＳトランジスタ４１と４２のゲート酸化膜はかかる動作電圧に応じた膜厚とされ、この実施例でも図４、５の従来例と同じく２５ｎｍと１５０ｎｍにそれぞれ設定される。

【００２５】ウェハ１０の半導体領域１１は半導体基板やエピタキシャル層やウェルであって、この例ではその表面にバッファ酸化膜１２が熱酸化により３５ｎｍの膜厚で付けられ、耐酸化性膜１３用に窒化シリコン膜がＣＶＤ法により１５０ｎｍの膜厚で成膜される。図１（ａ）の選択酸化工程では、耐酸化性膜１３を例えば図のように各トランジスタ領域を覆うパターンに形成した後にいわゆるＬＯＣＯＳ法による熱酸化を施すことにより、図示のように各領域を取り囲む素子分離膜ないしはフィールド酸化膜１４を６００～８００ｎｍ程度の膜厚で成膜する。

【００２６】図１（ｂ）は図１（ｃ）の第一酸化工程のための準備工程であって、図の左半分の薄いゲート酸化膜を付けるべき範囲を残して耐酸化性膜１３をフォトエッチングにより除去する。このためには、通常のフォトレジスト１９をマスクとして用いるフォトプロセスでフォトレジスト１９を図のように形成した上で例えば三フッ化窒素（NF_3）を含む雰囲気ガス内で耐酸化性膜１３をプラズマエッチングにより除去し、かつその下側のバッファ酸化膜１２を希フッ酸液による簡単なエッチングで除去して半導体領域１１の表面を露出させるのがよい。この図１（ｂ）の工程のフォトプロセスでは半導体領域１１の表面ないしバッファ酸化膜１２は耐酸化性膜１３によってフォトレジスト１９から隔てられているので、フォトレジスト１９と接触して汚染されるおそれはない。

【００２７】次の図１（ｃ）は第一酸化工程の状態を示す。この工程ではまず前の図１（ｂ）の状態からフォトレジスト１９をアッシング等の手段で除去して薄いゲート酸化膜を付けるべき図の左半分の範囲を耐酸化性膜１３で覆った状態で、右半分の半導体領域１１の表面を熱酸化して厚いゲート酸化膜２４を成膜する。このゲート酸化膜２４は通例のように水素と酸素のガス反応を利用するいわゆるパイロジェニック酸化法（以後パイロ酸化と称する）により成膜するのが成膜速度と膜質を高め得る点で有利である。この実施例では例えば９００℃、８０分程度のパイロ酸化条件で厚いゲート酸化膜２４を目標値の１５０ｎｍより厚めの１７０ｎｍの膜厚で成膜する。

【００２８】図１（ｄ）に示す次の第二酸化工程のための準備工程では図の左半分の範囲から耐酸化性膜１３とバッファ酸化膜１２を除去する。まず、耐酸化性膜１３の除去は厚いゲート酸化膜２４に影響を極力与えないように耐酸化性膜１３に対してできるだけ高い選択性をもつエッチング液を用いるウェットエッチングによるのがよく、特にこのエッチング液として熱燐酸を用いれば窒化シリコン膜からなる耐酸化性膜１３と厚いゲート酸化膜２４に対して２００：１程度の高いエッチング選択性が得られる。次のバッファ酸化膜１２は通例の希ふっ酸液によるウェットエッチングで除去することでよいが、この場合はエッチング選択性が全くないので前述の３５ｎｍの膜厚のバッファ酸化膜１２を除去する際に厚いゲート酸化膜２４の方も同じだけエッチングされて膜厚が１７０ｎｍから１３５ｎｍに減少する。なお、この図１（ｄ）の工程中に厚いゲート酸化膜２４は熱燐酸および希ふっ酸と接触するが、これらの無機酸との接触によって汚染を受けるおそれは周知のようにごく少ない。

【００２９】次の図１（ｅ）の第二酸化工程では前工程で耐酸化性膜１３とバッファ酸化膜１２とを除去して露出させた左半分の半導体領域１１の清浄な表面を熱酸化して薄いゲート酸化膜２３を付ける。この熱酸化にもパイロ酸化法を用いるのがよく、例えば８００℃、４０分程度の条件下で薄いゲート酸化膜２３を目標値の２５ｎｍの膜厚に成膜する。これと同時に厚いゲート酸化膜２４も積み増されるが膜厚が増すにつれ酸化膜の成長速度が落ちるので、薄いゲート酸化膜２３の成長より低い１５ｎｍ程度が積み増されて前工程の１３５ｎｍから目標値１５０ｎｍに近い膜厚になる。この後、減圧ＣＶＤ法により多結晶シリコン膜１５が堆積される。

【００３０】更に、同図（ｆ）ではフォトレジスト１９が塗布、パターニングされ、多結晶シリコン膜１５のフォトエッチングにより、ロジツク部２１のゲート電極２５と高耐圧部２２のゲート電極２６が形成される。以上

で本発明方法によるゲート酸化膜２３と２４の成膜およびゲート電極２５、２６の形成までが完了するが、図１（ｃ）の第一酸化工程と図１（ｅ）の第二酸化工程より前の図１（ａ）の耐酸化性膜１３がまだウェハ１０の表面にある状態で図１（ｂ）の準備工程でフォトエツチングを済ませてしまうので、フォトレジスト１９がゲート酸化膜２３や２４に接触し得ないことはもちろん、それらを成膜すべき範囲の半導体領域１１の表面にも接触しないので、清浄な半導体表面に不純物による汚染がないゲート酸化膜２３と２４を良好な膜質で容易に成膜することができる。

【００３１】参考のため、図２（ａ）および（ｂ）に、この後の工程における断面図を簡略に示す。図２（ａ）では、ゲート電極２５、２６およびフィールド酸化膜１４をマスクにして或いはフォトエッチング技術によるマスクによりｐ型の半導体領域１１の表面に高耐圧部２２のＭＯＳトランジスタ４２用にｎ型低濃度領域３２を拡散し、ロジック部２１および高耐圧部２２のＭＯＳトランジスタ４１、４２に対してｎ型ソース領域３３およびｎ型ドレイン領域３４と、ｐ型コンタクト領域３５を拡散する。この工程はゲート酸化膜２３、２４を残したまま行うことができる。

【００３２】最後に要所の酸化膜に窓開けをし、アルミニウム合金の電極３６を配設してソース端子Ｓとドレイン端子Ｄとゲート端子Ｇを導出する［図２（ｂ）］。このようにして、ウェハ１０に集積回路の回路要素の例として動作電圧が互いに異なるＭＯＳトランジスタ４１と４２を作り込むことができる。なお、ゲート電極２５、２６の上に層間絶縁膜が、電極３６の上に保護膜が実際にはそれぞれ設けられるが図では省略されている。

【００３３】本発明方法によりゲート酸化膜２３と２４を成膜したウェハ１０に図２のようにＭＯＳトランジスタ４１と４２を組み込んだ集積回路装置の試験結果では、従来では１～３％の確率で汚染が原因と思われるゲート耐圧やしきい値の不良が発生していたのに対し、本発明方法による場合は製造直後のかかる不良の発生確率はほぼ０であり、さらに加熱下の１００時間程度の劣化加速試験の結果でもゲート耐圧や動作特性の劣化は特に認められなかった。

【００３４】図３（ａ）ないし（ｆ）は本発明の別の製造方法の実施例の主な工程ごとの断面図である。図３（ａ）は、図１（ａ）と同様選択酸化工程の状態を示す。図は集積回路を作り込むべきウェハ１０のごく一部であり、図の右半分と左半分が図２に示されたＭＯＳトランジスタ４１と４２がそれぞれ作り込まれる領域である。

【００３５】ウェハ１０の半導体領域１１は半導体基板やエピタキシャル層やウェルであって、この例ではその表面にバッファ酸化膜１２が熱酸化により３５ｎｍの膜厚で付けられ、耐酸化性膜１３として窒化シリコン膜がプラズマＣＶＤ法により１５０ｎｍの膜厚で成膜される。図３（ａ）の選択酸化工程では、耐酸化性膜１３を例えば図のように各トランジスタ領域を覆うパターンに形成した後にいわゆるＬＯＣＯＳ法による熱酸化を施すことにより、図示のように各領域を取り囲む素子分離膜ないしはフィールド酸化膜１４を６００～８００ｎｍ程度の膜厚で成膜する。

【００３６】耐酸化性膜１３とバッファ酸化膜１４とを除去した後、９００℃、６１分程度のパイロ酸化によって１５０ｎｍの高耐圧部２２用の厚い酸化膜２４を成膜し、続いて減圧ＣＶＤ法により第一の多結晶シリコン膜１５を全面に堆積し、フォトレジスト１９を塗布し、高耐圧部２２上にパターン形成する〔図３（ｂ）〕。次に、ロジツク部２１上の第一の多結晶シリコン膜１５をエッチング除去した後、フォトレジスト１９を除去し、ふっ酸によりロジツク部２１上の厚いゲート酸化膜２６をエッチングして、半導体領域１１の表面を露出させる〔図３（ｃ）〕。高耐圧部２２上は多結晶シリコン膜１５があるため、ゲート酸化膜２４はエッチングされない。しかも高耐圧部２２上の第一の多結晶シリコン膜１５は、高耐圧部２２全体を覆うように残っているため、言い換えると高耐圧部２２上の第一の多結晶シリコン膜１５が、高耐圧部２２の活性領域より大きく残っているため、後でフォトエッチングにより形成されるゲート電極２６の直下の酸化膜のアンダーカットは起こらない。

【００３７】しかる後、第二のゲート酸化膜２３を８００℃、４０分程度のパイロ酸化により２５ｎｍの厚さに成膜する。このとき、高耐圧部２２の第一の多結晶シリコン膜１５も酸化され、その上に酸化膜１８が形成される。続いて、第二の多結晶シリコン膜１６を全面に堆積し、フォトレジスト１９を塗布し、ロジツク部２１上にパターン形成する〔図３（ｄ）〕。

【００３８】次に、高耐圧部２２の第二の多結晶シリコン膜１６をエッチング除去する。このとき、先に述べた高耐圧部２２の第一の多結晶シリコン膜１５の上の酸化膜１８がこのエッチングのエンドポイントディテクタとして働くので、高耐圧部２２の第一の多結晶シリコン膜１５はエッチングされない。フォトレジスト１９を除去し、必要があれば、第一の多結晶シリコン膜１５の上の酸化膜１８をこの時点でエッチングすることもできる〔図３（ｅ）〕。この状態では、ロジック部２１には第二の多結晶シリコン膜１６が、また高耐圧部２２には第一の多結晶シリコン膜１５が未加工の状態で存在する。必要があれば、多結晶シリコン膜１５、１６を低抵抗化するための不純物の導入を行う。ただし、この工程は多結晶シリコン膜を堆積するとき同時に不純物を導入するいわゆるドープド多結晶シリコン膜にするなら不要である。

【００３９】ついで、フォトレジスト１９を塗布し、パターン形成してロジツク部２１のゲート電極２５と高耐

圧部２２のゲート電極２６とを形成する〔図3（ｆ）〕。以上で本発明方法によるゲート酸化膜２３と２４の成膜およびゲート電極２５、２６の形成までが完了するが、以上の方法によっても、フォトレジスト１９を使用する工程の図３（ｃ）、（ｅ）において常にフォトレジスト１９の下に多結晶シリコン膜１５、１６があり、ゲート酸化膜２３、２４にフォトレジスト１９が触れて不純物汚染を引き起こすことがない。清浄な半導体表面に不純物による汚染がないゲート酸化膜２３と２４を良好な膜質で容易に成膜することができる。またゲート電極２５、２６の下のゲート酸化膜がアンダーカットされることもない。

【００４０】これ以降の工程は、図２（ａ）および（ｂ）に断面図で示したものと同じでよい。本発明方法によりゲート酸化膜２３と２４を成膜したウェハ１０に図2のようにＭＯＳトランジスタ４１と４２を組み込んだ集積回路装置の試験結果では、汚染やゲート電極下の酸化膜のアンダーカットが原因と思われるゲート耐圧やしきい値の不良がほぼ0であり、さらに加熱下の１００時間程度の劣化加速試験の結果でもゲート耐圧や動作特性の劣化は特に認められなかった。

【００４１】上記の例では、先に厚いゲート酸化膜２４を成膜し［図３（ｂ）］、その後薄いゲート酸化膜２３を成膜した［図３（ｄ）］。これを逆にして先に薄いゲート酸化膜２３を成膜し、後で厚いゲート酸化膜２４を成膜することもできるが、後の酸化時の一層目の多結晶シリコン膜１５の目減りを考慮すれば、先に厚いゲート酸化膜２４を成膜する方が有利である。

【００４２】なお、熱酸化はドライ酸化法やスチーム酸化法によることもできるが、いわゆるパイロジェニック酸化法によるのが成膜の速度を上げ膜圧の制御精度を高め得る上で最も有利である。

【００４３】

【発明の効果】以上説明したように本発明第一の方法では、集積回路を組み込むべきウェハに膜厚が異なるゲート酸化膜を成膜するため、まず選択酸化工程においてゲート酸化膜を成膜すべきすべての個所に耐酸化性膜を被覆した状態でウェハに熱酸化を施し、この耐酸化性膜を薄いゲート酸化膜の成膜個所に残した状態で第一酸化工程では熱酸化により厚いゲート酸化膜を成膜し、更に第二酸化工程では耐酸化性膜をすべて除去した状態で熱酸化により薄いゲート酸化膜を成膜し、また本発明第二の方法では、ゲート酸化膜を成膜すべきすべての個所に一方の膜厚のゲート酸化膜とゲート電極を加工すべき電極膜とを形成し、他方のゲート酸化膜を成膜すべきすべての個所の酸化膜と電極膜を除去し、ゲート酸化膜を成膜すべきすべての個所に他方の膜厚のゲート酸化膜とゲート電極を加工すべき電極膜とを形成し、二層の電極膜が形成された個所の上層の電極膜を除去することによって、次の効果が得られる。

【００４４】（ａ）フォトレジストを用いるフォトプロセスが、第一の方法ではゲート酸化膜の成膜個所がまだ耐酸化性膜で覆われている状態で、第二の方法では電極膜で覆われている状態で済ませるので、金属等の有害な不純物が含まれ易いフォトレジスト樹脂がゲート酸化膜はもちろんその成膜範囲のウェハ面にも接触し得ないので、ウェハの清浄な半導体の表面に不純物により汚染されないゲート酸化膜を良好な膜質で容易かつ確実に成膜することができる。

【００４５】（ｂ）ゲート電極直下のゲート酸化膜がふっ酸にさらされることがなく、ゲート電極直下のアンダカットもないため、デバイスの信頼性を低下させることがない。特に第一の方法においては、（ｃ）　従来とおなじ工程数で上述の効果が得られる。すなわち、従来は厚いゲート酸化膜の成膜工程と薄いゲート酸化膜の成膜工程との間にフォトエツチング工程を挿入していたのに対し、本発明方法では、選択酸化工程後の準備工程でフォトエツチングを施した後に第一酸化工程で厚いゲート酸化膜を、第二酸化工程で薄いゲート酸化膜をそれぞれ成膜するので、二回の酸化工程と一回のフォトエツチング工程とを経由する点で同じである。なお、周知のように選択酸化工程はどの集積回路にも一般的な工程なので本発明のために特に追加する必要はない。そして第一酸化工程のために耐酸化性膜を厚いゲート酸化膜の成膜個所からプラズマエッチング法により除去する本発明の実施態様は、ウェットエッチング法よりもフォトレジスト膜が損傷を受けるおそれを減少させてフォトエッチングを容易にする利点がある。また、第二酸化工程のために耐酸化性膜をそれに対して選択性を有するエッチング液、特に熱燐酸液を用いて薄いゲート酸化膜の成膜個所からウェットエッチングによって除去する態様は、厚いゲート酸化膜に与える影響を減少させてそれに正確な膜厚をもたせる効果を有する。

【図面の簡単な説明】

【図１】（ａ）ないし（ｆ）は本発明に係るＭＯＳ型集積回路装置の製造方法を説明するためのゲート電極形成までの主要工程ごとの断面図

【図２】（ａ）および（ｂ）は図１に続く本発明に係るＭＯＳ型集積回路装置の製造方法を説明するための主要工程ごとの断面図

【図３】（ａ）ないし（ｆ）は本発明に係るＭＯＳ型集積回路装置の別の製造方法を説明するためのゲート電極形成までの主要工程ごとの断面図

【図４】（ａ）ないし（ｆ）は従来のＭＯＳ型集積回路装置の製造方法を説明するためのゲート電極形成までの主要工程ごとの断面図

【図５】（ａ）ないし（ｆ）は従来のＭＯＳ型集積回路装置の別の製造方法を説明するためのゲート電極形成までの主要工程ごとの断面図

【符号の説明】

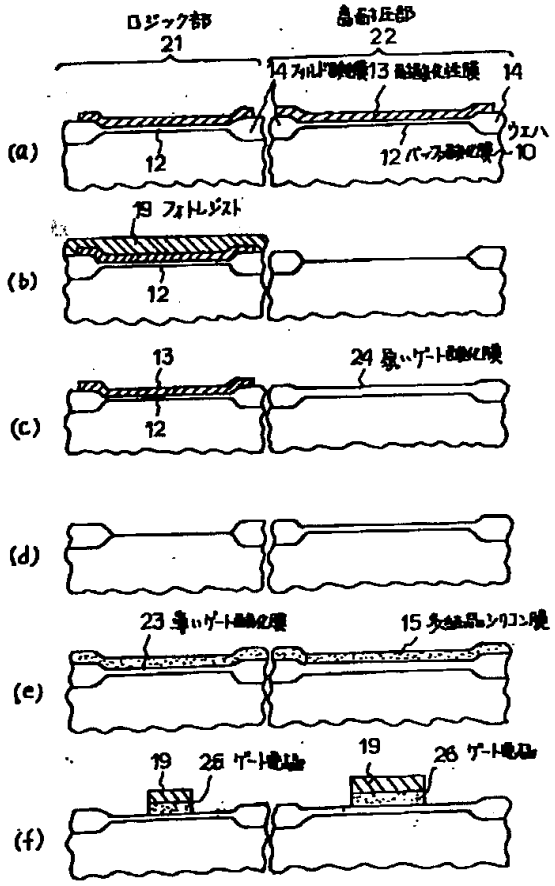
13

10	ウェハ
11	半導体領域
12	バッファ酸化膜
13	耐酸化性膜
14	フィールド酸化膜
15	第一の多結晶シリコン膜
16	第二の多結晶シリコン膜
17	第一酸化膜
18	多結晶シリコン膜上酸化膜
19	フォトレジスト
21	ロジツク部
22	高耐圧部

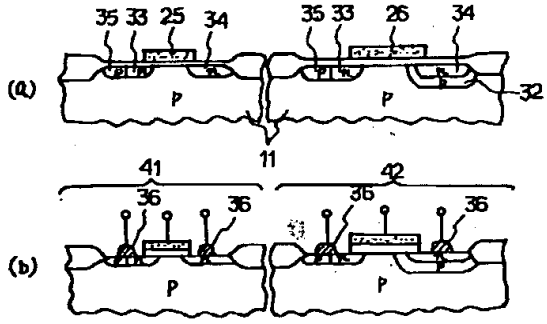
14

23	薄いゲート酸化膜
24	厚いゲート酸化膜
25	ゲート電極
26	ゲート電極
32	n型低濃度領域
33	n型ソース領域
34	n型ドレイン領域
35	p型コンタクト領域
36	電極
41	ロジック部のMOSトランジスタ
42	高耐圧部のMOSトランジスタ

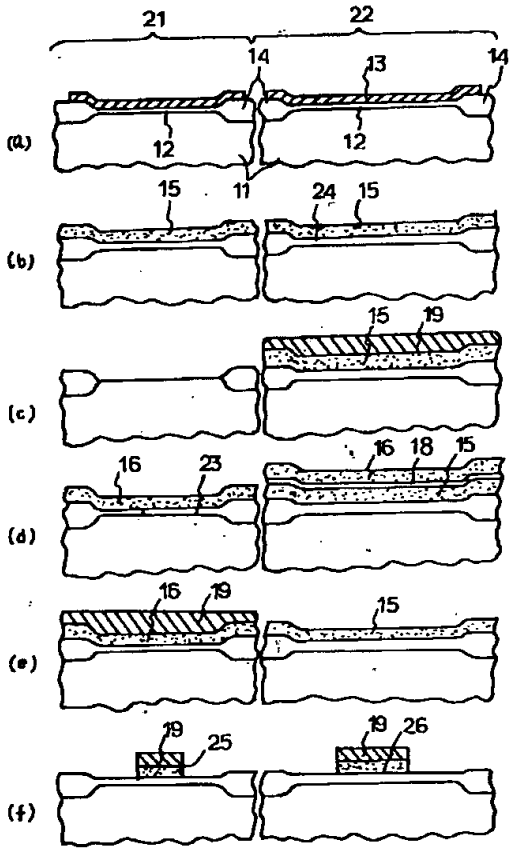
【図1】



【図2】



【図3】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(e)
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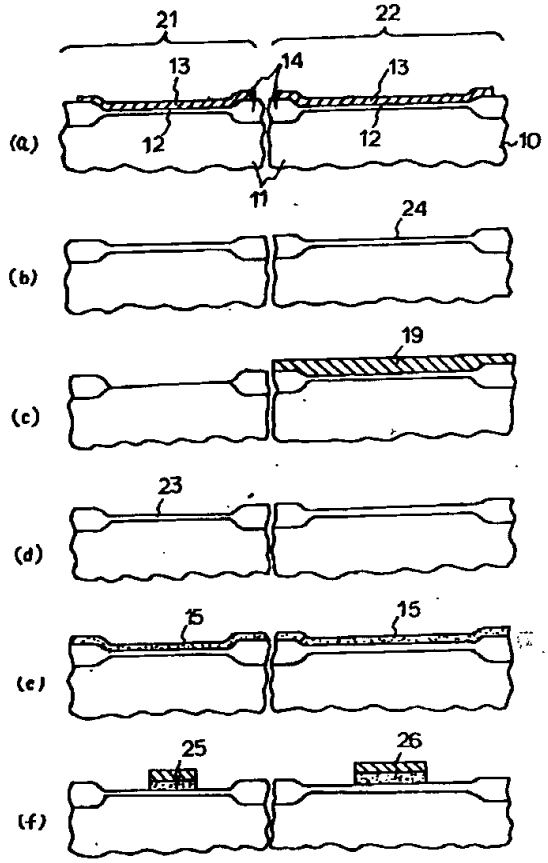
(f)

【図4】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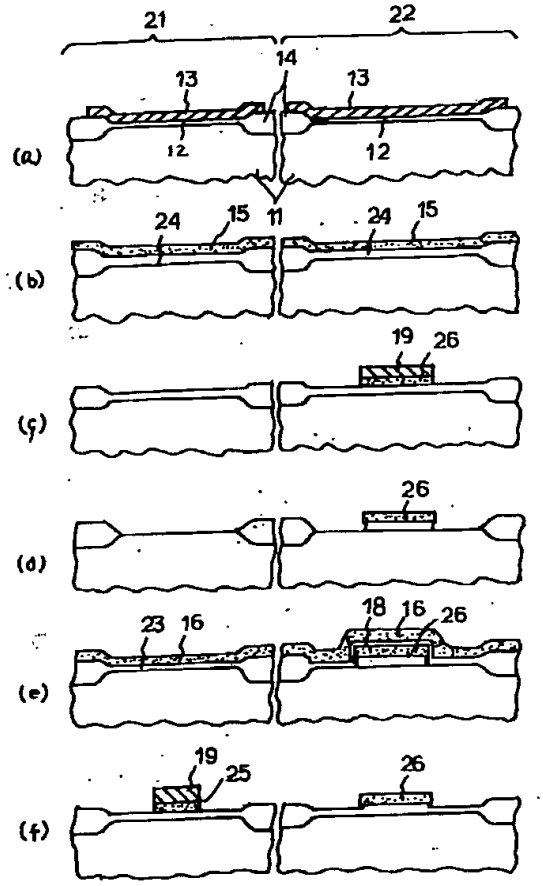
【図5】



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(51)Int.Cl.⁶	識別記号	庁内整理番号	FI		技術表示箇所
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				301 P	